REMARKS

In the office action dated March 26, 1997, the Examiner rejected all of Applicants' claims under 35 USC §112, second paragraph. In particular, the Examiner stated that the claims recite that the buffer is connected between a parallel side and a serial side, but fails to recite how the data flows through those two sides to reach the buffer and the network link. In addition, the Examiner rejected all of Applicants' claims under 35 USC §103 as being unpatentable over U.S. Patent No. 5, 485,584 issued to Hausman, et al. ("Hausman") in view of U.S. Patent No. 5, 179,661 issued to Copeland, et al. ("Copeland").

In response to the Examiner's rejections, Applicants have cancelled claims 1 - 21 and added new claims 22 - 39. Claims 22 - 39 are pending and submitted for reconsideration.

Applicants believe that their new claims avoid the Examiner's rejection under 35 USC §112, second paragraph, and the withdrawal of that rejection is respectfully requested.

Turning now to the Examiner's rejections under 35 U.S.C. § 103, Hausman deals generally with network controllers (called LAN adapters in Hausman) and in particular seeks to minimize latency. Hausman teaches the reduction of latency in three ways: (1) by generating interrupts before complete packets of data have been received from the network so that reception of the remainder of the packet overlaps with the host computer interrupt latency; (2) by generating a second early interrupt during the reception of large packets so that the copying of the packet to the host may overlap the reception of the final portion of the packet; and (3) by allowing the adapter to begin packet transmission before the packet is completely transferred from the host to the adapter (column 1, lines 40-60).

Copeland deals generally with a serial communications controller with a very small buffer memory, (16 bytes). The problem that Copeland seeks to solve is the loss of data if the host computer cannot respond quickly to a serial controller interrupt and the buffer overflows, (column 1, lines 22-42). Prior art systems, according to Copeland, attempt to solve this problem with a technique called "data flow control" in which a software program signals the remote transmitter to halt the output of data until the host computer catches up with the data stored in the buffer. This is done by driving the Data Terminal Ready or the Request to Send lines of the serial card to a "not ready" status to halt the flow of serial data from the remote transmitter, (column 2, lines 7-16). The problem with this approach according to Copeland is that it is sometimes too slow, (column 2, lines 17-24). Copeland's solution is to use two signals in the UART to control the remote transmitter rather than relying on the host computer software, (column 2, lines 48 - 60).

Applicants submit that Copeland is not relevant since it deals with data loss from a small buffer overflow whereas Applicants' are improving speed of transmission and not solving a lost data problem.

Applicants invention deals with network controllers as does Hausman. However, Applicants' invention assumes that the solutions taught by Hausman have already been implemented (see Applicants' Figure 2) and move on to make yet a further, more sophisticated improvement not taught or suggested by Hausman. That is, Applicants address a problem of optimizing the transmission of data from the host computer to the buffer memory. As pointed out by Applicants on page 4-7, the activities of the parallel side and serial side are intimately connected in the prior art. That is, the timing of data transfers from main memory to the buffer are dependent on receiving a transmission complete signal. And as pointed out on page 7 of Applicants specification, this leads to CPU idle time with respect to data transmission. Applicants solve this problem by further decoupling the data transfer

into the buffer memory from the host from the data transfer out of the buffer memory onto the network. Please note that the desirability or possibility of such an approach is neither mentioned not taught by Hausman. In particular, Applicants claim 22 is limited to

copying data to be transmitted over a network from a main memory in a host computer to a buffer memory in a network controller for so long as unused memory locations remain in said buffer memory;

allocating memory locations in said buffer memory as being available for new frame data to be copied form said main memory upon successful transfer of a predetermined quantity of said data from said buffer memory over said physical link.

The limitation "copying data to be transmitted over a network from a main memory in a host computer to a buffer memory in a network controller for so long as unused memory locations remain in said buffer memory " is intended to make it clear that the parallel side of the controller is decoupled from the serial side except for the unused buffer memory locations. That is, the host will load the buffer continuously for so long as there are unused memory locations. And, memory locations are made available by the serial side by reallocating the space occupied by the most recently sent data which is set out in the limitation:

> "allocating memory locations in said buffer memory as being available for new frame data to be copied form said main memory upon successful transfer of a predetermined quantity of said data from said buffer memory over said physical link"

Since neither Hausman nor Copeland teach or suggest such an approach, Applicants submit that their claim 22 is allowable and such action is respectfully requested.

Claim 24 further defines the mechanism of how the data copy to the buffer memory is kept continuous for so long as there is available memory location in the buffer. As pointed

out in Applicants specification this is accomplished by sending a transmission complete signal to the host after completion of a copy to buffer regardless of whether the frame has in fact been successfully sent over the network. Again, since neither Hausman nor Copeland teach or suggest such an approach, Applicants submit that their claim 22 is allowable and such action is respectfully requested.

Claims 25-28 are dependent on claim 22 and are believed to be allowable for the same reasons as set out in claim 22 and such action is respectfully requested.

Independent claim 29 is a system claim that includes the limitation:

> "a controller for controlling the operation of said network controller including supplying a frame transmit complete indication to said CPU immediately after the copying of a complete frame from said main memory to said buffer memory but prior to the actual complete transmission of said frame over the network, for commencing transmission of said data over said network upon receipt of a threshold quantity of data into said buffer memory from said main memory, and for causing buffer memory locations occupied by successfully transmitted frames to become available for data to be copied from said main memory"

This limitation makes it clear that the frame transmit complete indication is sent to the CPU prior to the actual complete transmission of the frame over the network. Accordingly, Applicants submit that the arguments set out in connection with claims 22 and 24 are applicable and the allowance of claim 29 is respectfully requested.

Claims 30-36 are dependent on claim 29 are submitted to be allowable for the same reasons.

Independent claim 37 includes the limitations on the parallel side:

if yes, indicating to said driver layer that said data frame has been successfully transmitted;

and on the serial side:

d. if yes, indicate transmission complete to said parallel side and wait for next data frame written to said buffer memory

Again, these limitation are intended to define the unique combination that Applicants submit is their invention and which are not taught or suggested by the prior art of record. Accordingly, Applicants submit that their claim 37 is allowable and such action is respectfully requested. Claims 38 and 39 which are dependent on claim 37 are submitted to be allowable for the same reasons as set out in claims 37 and such action is respectfully requested.

In this communication, Applicants have amended their specification cancelled certain claims, added new claims and pointed out how their pending claims as amended are allowable over the prior art of record. Accordingly, Applicants believe that this application is in condition for allowance and such action is courteously solicited.

If there are any additional charges, please charge them to our Deposit Account Number 02-2666. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact Jim H. Salter at (408) 720-8598.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Dated: 7/28, 1997

James H. Salter
Registration No. 35,668

Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8598

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

on July 28, 1997
Date of Deposit

Anna Morris
Name of Person Mailing Correspondence

Signature 7-28-97
Date